AMENDMENTS TO THE CLAIMS:

The following listing of claims will replace all prior versions of claims in the application:

1. (Currently Amended) A receiver for boundary scan testing of differential interconnections between the receiver and a transmitter, the receiver comprising:

an input test buffer having differential null detection capability and a common mode reference voltage; and

an interface mechanism for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing.

2. (Original) The receiver as defined in claim 1, wherein the interface mechanism comprises a plurality of detectors for generating data and fault indicator signals.

3. (Original) The receiver as defined in claim 2, wherein the interface mechanism further comprises a technology mapper for processing the one or more output signals from the input test buffer into one or more suitable input signals for the interface mechanism.

4. (Original) The receiver as defined in claim 2, wherein the interface mechanism further comprises an integrator for processing the data and fault indicator signals of the detectors into one or more suitable output signals for the interface mechanism.

5. (Original) The receiver as defined in claim 2, wherein one of the plurality of detectors is a signal recoverer for recovery of the test data signal from the transmitter.

6. (Original) The receiver as defined in claim 2, wherein one of the plurality of detectors is an AC short/null detector.

7. (Original) The receiver as defined in claim 2, wherein one of the plurality of detectors is a DC short detector.

8. (Original) The receiver as defined in claim 2, wherein one of the plurality of detectors is an AC detector.

9. (Original) The receiver as defined in claim 2, wherein one of the plurality of detectors is a heterogeneous capacitor detector.

10. (Original) The receiver as defined in claim 9, wherein the heterogeneous capacitor detector comprises a first flip-flop for sampling a first signal on an even test clock signal, a second flip-flop for sampling a second signal on an odd test clock signal, and a logic gate for combining the outputs of the first and second flip-flops.

11. (Currently Amended) An interface mechanism for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing of differential interconnections between a receiver and a transmitter, the receiver includes an input test buffer having differential null detection capability and a common mode reference voltage and the output of the input test buffer is coupled to the input of the interface mechanism, the interface mechanism comprising:

a plurality of detectors for generating data and fault indicator signals; and

an integrator for processing the data and fault indicator signals of the plurality of detectors into one or more suitable output signals for the interface mechanism.

12. (Original) The interface mechanism as defined in claim 11, further comprising a technology mapper for processing the one or more output signals from the input test buffer into one or more suitable input signals for the interface mechanism.

13. (Canceled)

14. (Original) The interface mechanism as defined in claim 11, wherein one of the plurality of detectors is a signal recoverer for recovery of the test data signal from the transmitter.

15. (Original) The interface mechanism as defined in claim 11, wherein one of the plurality of detectors is an AC short/null detector.

16. (Original) The interface mechanism as defined in claim 11, wherein one of the plurality of detectors is a DC short detector.

17. (Original) The interface mechanism as defined in claim 11, wherein one of the plurality of detectors is an AC detector.

18. (Original) The interface mechanism as defined in claim 11, wherein one of the plurality of detectors is a heterogeneous capacitor detector.

19. (Original) The interface mechanism as defined in claim 18, wherein the heterogeneous capacitor detector comprises a first flip-flop for sampling a first signal on an even test clock signal, a second flip-flop for sampling a second signal on an odd test clock signal, and a logic gate for combining the outputs of the first and second flip-flops.

20. (Currently Amended) A method for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing of differential interconnections between a receiver and a transmitter, the method comprising:

receiving an analog differential test signal pair;

converting the analog differential test signal pair into a digital differential test signal pair; and

detecting a differential null condition in the digital differential test signal pair indicating that one of the five fault syndromes has occurred,

wherein detecting includes utilization of a common mode reference voltage.

21. (Currently Amended) An apparatus for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing of differential interconnections between a receiver and a transmitter, the apparatus comprising:

means for receiving an analog differential test signal pair;

means for converting the analog differential test signal pair into a digital differential test signal pair; and

means for detecting a differential null condition in the digital differential test signal pair indicating that one of the five fault syndromes has occurred,

wherein detecting includes utilization of a common mode reference voltage.